IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor integrated circuit comprising:

an internal main bus;

first and second microprocessors sharing said internal main bus;

a first debug serial bus with one end thereof connected to said first microprocessor;

a second debug serial bus with one end thereof connected to said second microprocessor; ~~and~~

a debugging module connected to the other ends of said first and second debug serial buses and transferring at least a debugging program and debugging data to said first microprocessor via said first debug serial bus and to said second microprocessor via said second debug serial bus;

a first debug supporting unit provided in said first microprocessor and controlling a debugging function of said first microprocessor;

a second debug supporting unit provided in said second microprocessor and controlling a debugging function of said second microprocessor;

a first debug controlling bus which connects said first debug supporting unit and said debugging module; and

a second debug controlling bus which connects said second debug supporting unit and said debugging module.

2. (Original) The semiconductor integrated circuit of claim 1 further comprising a dedicated external debugging terminal which connects said debugging module and a debugging tool for controlling a debugging task in accordance with a debugging program.

3. (Original) The semiconductor integrated circuit of claim 1, wherein said debugging module is directly connected to said internal main bus.

4. (Currently amended) The semiconductor integrated circuit of claim 2, wherein said debugging module is directly connected to said internal main bus, and said debugging module carries out directly ~~the~~ a memory access which said debugging tool sends for a memory device connected to said internal main bus.

5. (Original) The semiconductor integrated circuit of claim 1 further comprising a memory controller, a direct memory access controller and an input / output controller, all of which are connected to said internal main bus.

6. (Canceled)

7. (Canceled)

8. (Currently Amended) The semiconductor integrated circuit of claim [[7]] 5, wherein said debugging module comprises:

an external debug interface connected to an external debugging tool;

a multi - debug control register connected to said external debug interface and said first and second microprocessors;

a debug control register, an address register, a byte enabling register and a data register, all of which are connected to said external debug interface;

a debug serial bus converting circuit connected to said debugging control register;

a debug serial bus selector connected to said multi - debug control register, said debug serial bus converting circuit and said first and second debug serial buses; and

an internal direct memory access controller connected to said debug control register, said address register, said byte enabling register, said data register and said internal main bus.

9. (Currently Amended) The semiconductor integrated circuit of claim [[6]] 1, wherein said debugging module monitors not only a debug state of said first microprocessor via said first debug controlling bus but also a debug state of said second microprocessor via said second debug controlling bus, and demands debugging interruption signal for shifting to a debugging mode.

10. (Currently Amended) The semiconductor integrated circuit of claim [[7]] 5, wherein said debugging module monitors not only a debug state of said first microprocessor via said first debug controlling bus but also a debug state of said second microprocessor via said second debug controlling bus, and demands debugging interruption signal for shifting to a debugging mode.

11. (Original) The semiconductor integrated circuit of claim 8, wherein said debugging module monitors not only a debug state of said first microprocessor via said first debug controlling bus but also a debug state of said second microprocessor via said second debug controlling bus, and demands debugging interruption signal for shifting to a debugging mode.

12. (Original) The semiconductor integrated circuit of claim 1, wherein said debugging module optionally demands each of said first and second microprocessors to delay returning to a user mode from a debugging mode.

13. (Original) The semiconductor integrated circuit of claim 1, wherein: said first microprocessor comprises a first bus interface unit connected not only to a microprocessor core thereof but also to said first debug serial bus and said internal main bus; and said second microprocessor comprises a second bus interface unit connected not only to a microprocessor core thereof but also to said second debug serial bus and said internal main bus.

14. (Original) The semiconductor integrated circuit of claim 13, wherein:

said first bus interface unit comprises an internal main bus / debug serial bus controlling circuit connected to said debugging module and said microprocessor core, a parallel - to - serial converting circuit connected to said debugging module and said internal main bus / debug serial bus controlling circuit, a serial - to - parallel converting circuit connected to said debugging module and said parallel - to - serial converting circuit, and a selector connected to said microprocessor core, said internal main bus / debug serial bus controlling circuit, said parallel - to - serial converting circuit and said serial - to - parallel converting circuit; and

said second bus interface unit comprises an internal main bus / debug serial bus controlling circuit connected to said debugging module and said microprocessor core, a parallel - to - serial converting circuit connected to said debugging module and said main bus / debug serial bus controlling circuit, a serial - to - parallel converting circuit connected to said debugging module and said parallel - to - serial converting circuit, and a selector connected to said microprocessor core, said internal main bus / debug serial bas controlling circuit, said parallel - to - serial converting circuit and said serial - to - parallel converting circuit.

15. (Currently Amended) A system board comprising:

a wiring board;

a semiconductor integrated circuit which comprises an internal main bus, first and second microprocessors sharing said internal main bus, a first debug serial bus with one end thereof connected to said first microprocessor, a second debug serial bus with one end thereof connected to said second microprocessor, and a debugging module connected to the other ends of said first and second debug serial buses and transferring at least a debugging program and debugging data to said first microprocessor via said first debug serial bus, and to said second microprocessor via said second debug serial bus; ~~and~~

a memory mounted on said wiring board and storing at least debugging data;

a memory mounted on said wiring board and storing at least debugging data;

a first debug supporting unit provided in said first microprocessor and controlling a debugging function of said first microprocessor; and

a second debug supporting unit provided in said second microprocessor and controlling a debugging function of said second microprocessor;

a first debug controlling bus which connects said first debug supporting unit and said debugging module; and

a second debug controlling bus which connects said second debugging support unit and said debugging module.

16. (Original) The system board of claim 15 further comprising an input / output interface circuit mounted on said wiring board.

17. (Original) The system board of claim 15 further comprising a dedicated debug interface terminal which connects said debugging module of said semiconductor integrated circuit and a debugging tool for controlling a debugging operation in accordance with a debugging program.

18. (Original) The system board of claim 15, wherein said semiconductor integrated circuit further comprises a memory controller, a direct memory access controller and an input / output controller, all of which are connected to said internal main bus.

19. (Canceled)

20. (Currently Amended) A debugging system comprising:

a wiring board;

a semiconductor integrated circuit which is mounted on said wiring board and comprises: an internal main bus; first and second microprocessors sharing said main internal bus; a first debug serial bus with one end thereof connected to said first microprocessor; a second debug serial bus with one end thereof connected to said second microprocessor; and a debugging module connected to the other ends of said first and second debug serial buses and transferring at least a debugging program and debugging data to said first microprocessor via said first debug serial bus, and to said second microprocessor via said second debug serial bus;

a memory mounted on said wiring board and storing at least debugging data; and

a debugging tool connected to said debugging module of said semiconductor integrated circuit;

a first debug supporting unit provided in said first microprocessor and controlling a debugging function of said first microprocessor; and

a second debug supporting unit provided in said second microprocessor and controlling a debugging function of said second microprocessor;

a first debug controlling bus which connects said first debug supporting unit and said debugging module; and

a second debug controlling bus which connects said second debug supporting unit and said debugging module.

21. (Original) The debugging system of claim 20, wherein said semiconductor integrated circuit further comprises a memory controller, a direct memory access controller and an input / output controller, all of which are connected to said internal main bus.

22. (Canceled)